REMARKS

Claims 1-31 and 96 are currently pending in the application.

35 U.S.C. § 103 Rejections:

Claims 1, 6-10, 15-19, 28-31 and 96 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Stancil, U.S. Patent 7,149,927, in view of Luke, U.S. Patent 6,505,267 and in further view of Steely, U.S. Patetnt 5,581,719. Applicant respectfully traverses this rejection.

The cited references, taken singly or in combination, fail to teach or suggest all of the elements of the independent claims. Independent claim 1 recites, in pertinent part:

> "An SMBus host controller comprising
>
> a memory storing microcode comprising at least two programs each for handling a bus command protocol, each program comprising at least one instruction; ...
> a finite-state machine configured to receive and interpret the instructions read by said instruction fetch unit and manage the data transfer between the SMBus interface and a register set **in compliance with** said instructions read from said memory; ... and
> an address register array comprising a plurality of starting addresses of programs stored in said memory, said register comprising an offset for pointing at a specific register in said address register array (Emphasis added).

Independent claims 10 and 19 recite similar combinations of features.

In the office action, the Examiner contends that Stancil teaches an SMBus host controller including a finite-state machine configured to manage data transfer between the SMBus interface and an integrated electronic device. The Examiner cites Stancil at

Fig. 2, elements 112 and 116 and col. 4, lines 20-32 in support of this contention. Applicant notes that the Examiner is silent with regard to the a finite state machine configured to "interpret the instructions read by said instruction fetch unit" and further configured to "manage the data transfer ... in compliance with said instructions read from said memory." Col. 4, lines 14-32 of Stancil state the following:

> FIGS. 2-5 provide further detail regarding SMBus-to-JTAG emulator 110 pertaining to how the emulator converts between SMBus and JTAG. A more detailed block diagram of emulator 110 is shown in FIG. 2. As shown therein, the emulator 110 preferably comprises an SMBUs state machine 112, an SMBus packet decoder/encoder 114 and a JTAG interface logic state machine 116. The SMBus state machine 112 comprises logic that receives SMBus packets from the host test system 102 and, with the help of the SMBus packet decoder/encoder 114, extracts the information from the packets necessary for the JTAG logic 122. The decoder/encoder 114 then creates JTAG-compliant communications that are sent to the JTAG logic 122 associated with the DUT 120 under the control of the JTAG interface logic state machine 116. Similarly, JTAG communications from the JTAG logic 122 are received by state machine 116, decoded by decoder/encoder 114 and are converted to SMBus-compliant packets by decoder/encoder 114 and provided to the host test system 102 under the control of the SMBus state machine 112. (Emphasis added).

Nothing in the above citation teaches or suggests that state machine 112 and/or state machine 116 is configured to "interpret the instructions read by said instruction fetch unit" and further configured to "manage the data transfer ... in compliance with said instructions read from said memory." Furthermore, neither Luke nor Steely provide any teaching or suggestion that would remedy this deficiency in Stancil. Accordingly, the cited references, taken singly or in combination, fail to teach or suggest "a finite-state machine configured to receive and interpret the instructions read by said instruction fetch unit and manage the data transfer between the SMBus interface and a register set in compliance with said instructions read from said memory" as recited in claim 1 and similarly recited in the other ones of the independent claims.

For at least the reasons given above, Applicant submits that Stancil in view of Luke and in further view of Steely fails to teach or suggest all of the elements of the

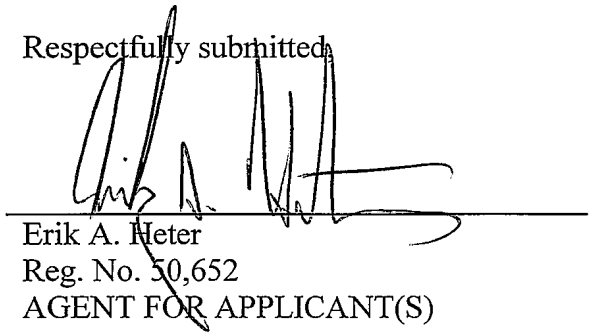
independent claims, as well as their associated dependent claims. Accordingly, removal of the 35 U.S.C. § 103(a) rejection is respectfully requested.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-92201/EAH.

Respectfully submitted,



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